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On the Design of a Modular Plug-and-Play Satellite Communication System

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Abstract

The growing demand of innovative modular communication systems is a driving factor towards designing a communication system that is easily developed, configured, modified, and expanded. To begin with, a communication system shall be able to establish a link between the satellite and ground station(s). From the space segment, the communication system shall be able to interface with the ground station(s) to be able to download telemetries as well as payload data no matter the number of payloads. Nevertheless, the communication system shall be able to receive uplink telecommands from any applicable authorized ground station(s). The main pillars of a modular communication system are: data rate, modulation scheme, RF output power, and data interface. The design attains the pillars by having the capability of configuring the data rate, modulation scheme, RF output power, and data interface. The design is fully implemented using COTS components and compartmentalized on different boards to enable plug-and-play as well as ease of expansion. The data rate and modulation scheme are configured through software while the RF output power can be fine tuned and course tuned using a DAC controlled by command in-flight or pre-set before flight, respectively. The data interface is customized according to user preference. This paper details the design, results, and optimization of a modular satellite communication system. The paper begins with design methodology, results and discussion, design optimization, and conclusion.

Keywords:

Commercial Off the Shelf (COTS), Data Rate, Modular, Output Power, Radio Frequency, UHF Transmitter, VHF Receiver

Acronyms/Abbreviations

Binary Phase Shift Keying (BPSK), Commercial Off the Shelf (COTS), Digital to Analog Converter (DAC), Electric Ground Support Equipment (EGSE), High Power Amplifier (HPA), International Telecommunication Union (ITU), Low Noise Amplifier (LNA), On Board Computer (OBC), Ultra High Frequency (UHF), Very Low Frequency (VHF)

1. Introduction

This paper highlights the design and development of a UHF transmit/VHF receive satellite communication system along with a presentation of its results and optimizations. The outline of this paper begins with a design methodology, followed by results and discussion, design optimization, and conclusion.

With the advancement in satellite communication and the need for smaller, faster, and less power consuming units comes the need to develop lightweight, simple, and adaptable designs. The main pillars of a communication system are data rate, RF output power, and modulation scheme. The main key is to develop a system in which the data rate, RF output power, and modulation scheme can be controlled and selected per mission without the need to change the design significantly. In other words, the purpose would be to allow reusability and adaptability thereby reducing development time and design effort. As a result, this is an advantage in terms of cost and development time [1].

As illustrated in Fig. 1 below, the main pillars of a communication system are data rate, RF output power, and modulation scheme. The pillars are related in the sense that different frequency bands have differed allocated bandwidth allotted to be used as per the International Telecommunication Union (ITU) radio regulations. Additionally, different modulation schemes consume a different amount of bandwidth depending on the data rate.

Finally, the required RF output power is calculated to meet the required link margin, considering the data rate, modulation scheme, and frequency band in use [2].

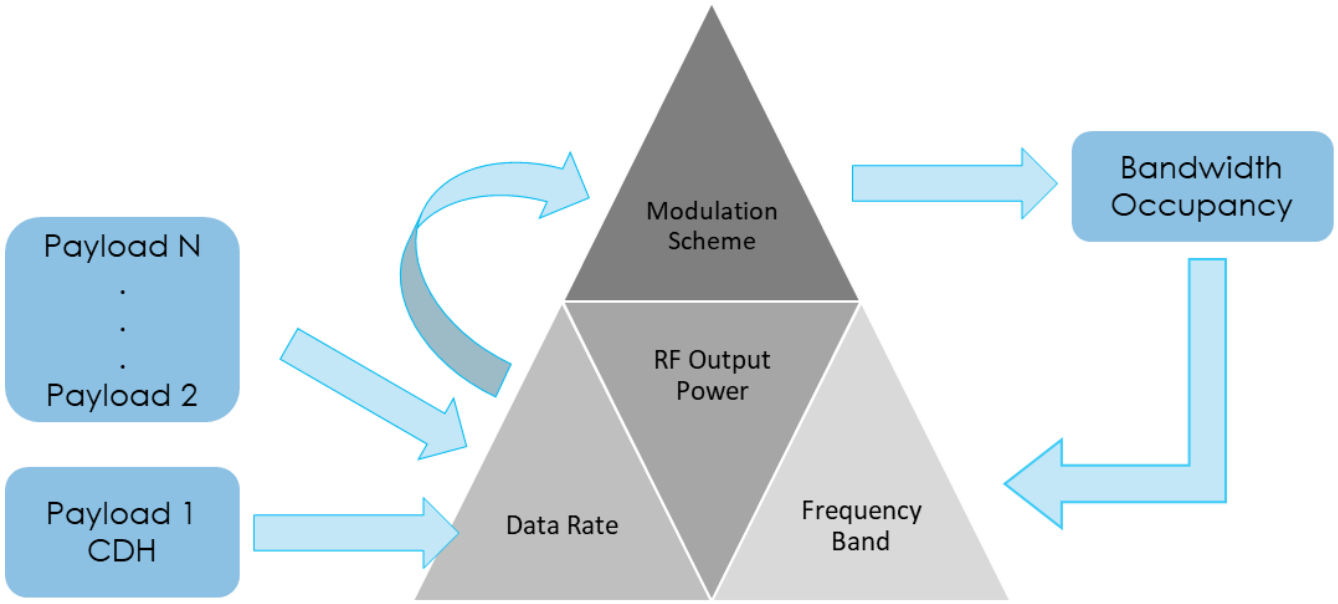

Fig. 1. Pillars of Modular Communication System

2. Design Methodology

The methodology behind which the modular communication system is designed is simple. Basically, the design is required to support different modulation schemes, data rates, frequency bands, and RF output power. The specification of the system is summarized in section 2.1 below.

2.1 Specification

As described in Table 1 below, the frequency range supported by the system is from 27-1050MHz. This covers the medium frequency (MF), high frequency (HF), very high frequency (VHF), and ultra high frequency (UHF) bands. The system has been verified and tested with frequency bands of operation of UHF downlink and VHF uplink. However, is flexible to be modified according to user preference and mission requirements.

Further, the data rate achievable using the system is 0.1 kbps up to 125kbps. However, the system has been verified and tested with 9.6kbps and 32kbps using Binary Phase Shift Keying (BPSK) modulation scheme.

Table 1. Specifications

Item	Specification
Frequency	27−1050 MHz Range
Data Rate	0.1 to 125 kbps
Modulation Scheme	FSK, MSK, 4FSK, GFSK, GMSK, ASK, AFSK, FM, and PSK
RF Output Power	Up to 1.2W
Data Interface	SPI for Uplink and Downlink Data I2C for Telemetry and Commands
Power Interface	+5V
Power Consumption	6.3W Full Duplex TX+RX Operation
Dimension	96.4mm x 91.1mm x 12mm
Transmission Mode	Full Duplex

The RF output power has been tested and verified up to 1.2W. There are two methods to configure the RF output power. The first method is directly by fixing the control voltage of the high power amplifier (HPA) to yield the desired RF output. The fixed voltage is supplied from the output of an adjustable voltage regulator and the RF output power in this case is course tuned. The second method is to supply the control voltage input with a digital to analog

converter (DAC) output. Hence, in this way, the RF output power is fine tuned and controlled by a command through software in-flight.

The following section 2.2 illustrates the block diagram and further elaborates on the constituents of the system.

2.2 Block Diagram

The system consists of UHF transmitter, high power amplifier (HPA), bi-directional coupler, UHF antenna, VHF receiver, low noise amplifier (LNA), and VHF antenna. The UHF transmitter and VHF receiver are placed on the same 1U standard PC104 PCB size. The UHF transmitter consists of a transceiver configured as a transmitter and an RF microcontroller to configure and setup the transmitter as well as receive data to be transmitted from the on board computer (OBC) via serial peripheral interface (SPI). The VHF receiver consists of a transceiver configured as a receiver and an RF microcontroller to configure and setup the receiver which sends received data to the on board computer (OBC) via serial peripheral interface (SPI). The transceiver board also includes other functions such as power conditioning, housekeeping, and serves as the digital interface with the on board computer (OBC).

Further, the RF front end components and circuitry are on another 1U standard PC104 PCB size. This board consists of high power amplifier (HPA), bi-directional coupler, low noise amplifier (LNA), as well as an optional filter. The high power amplifier (HPA) accepts a supply voltage as well as a control voltage to control the output power levels. The control voltage supply is two of each option, either direct fixed supply from an adjustable voltage regulator or through a DAC whose output can be set by command to yield the desired RF output power. The second option of using a DAC permits the in-flight reconfiguration of the power level. Moreover, the RF front end board also consists of a bi-directional coupler to measure the forward and reverse powers and record them as a telemetry with the aid of a logarithmic amplifier. Additionally, the RF front end also contains a low noise amplifier (LNA) to amplify the weakly received signal from ground station and an optional filter that can be mounted for UHF downlink or VHF uplink, if needed.

Fig. 2 below illustrates the block diagram of the system as described above.

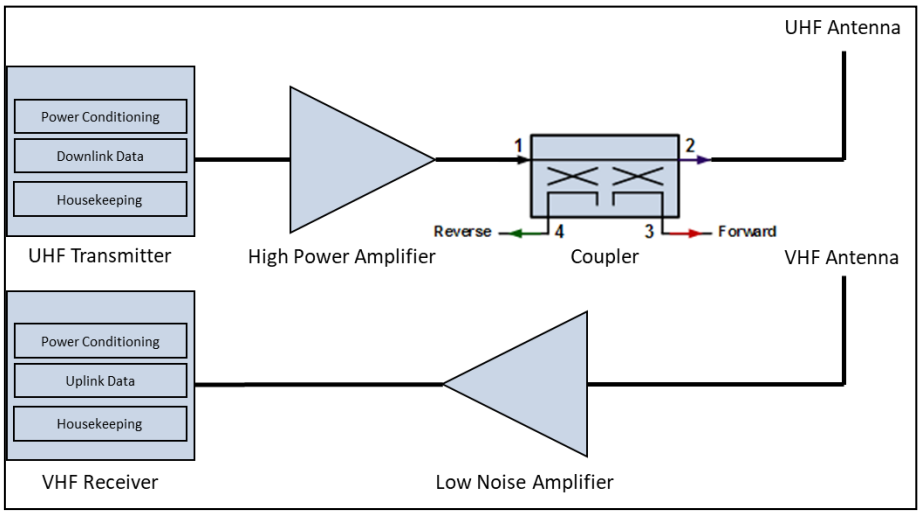

Fig. 2. Block Diagram

2.3 PCB Design

The system consists of two PCBs. Both PCBs are of the standard 1U PC104 size in terms of dimensions. However, instead of having a stacking connector, the connectors between the boards are customized. The first PCB is the transceiver PCB and encompasses the UHF and VHF transceivers as well as power conditioning and housekeeping circuitry. The second PCB is the RF front end PCB and contains the RF front end components such as high power amplifier (HPA), low noise amplifier (LNA), and bi-directional coupler as well as an optional filter.

Fig. 3 below illustrates the top view of the transceiver. It consists of UHF transmitter, VHF Receiver, transmitter RF microcontroller, and receiver RF microcontroller covered with an EMI Shield.

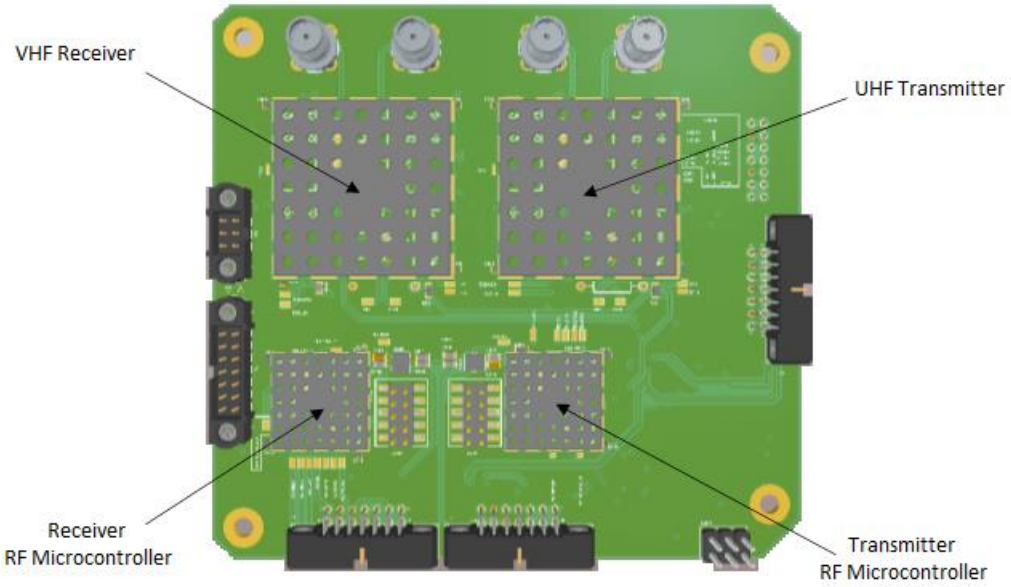

Fig. 3. Transceiver Board (Top View)

Fig. 4 below illustrates the bottom view of the transceiver. It consists of power conditioning circuitry that regulate the input voltage to supply the components of the transceiver and RF front end. It also contains housekeeping circuitry that gather all of the communication subsystem telemetries and transfers them to the on board computer (OBC) via I2C data interface.

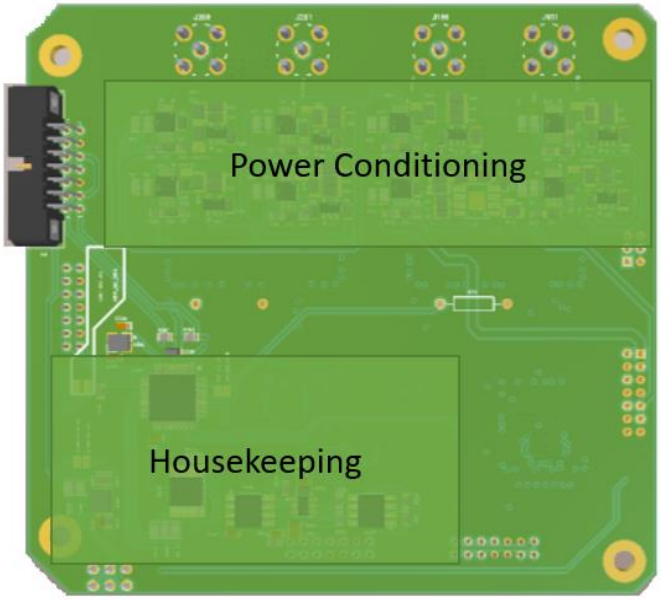

Fig. 4. Transceiver Board (Bottom View)

Fig. 5 below illustrates the top view of the RF front end. It illustrates the constituents of the RF front end. Each section is basically a small PCB incorporated on a larger PC104 size PCB. Each section has its own connector for ease of design adaptability and 4 mounting holes that aid in design flexibility such as mounting a heat sink or stacking multiples of each constituent, such as HPA, LNA, Filter, etc in the form of smaller PCBs. This can be useful to adapt the configurations or implement selective redundancy.

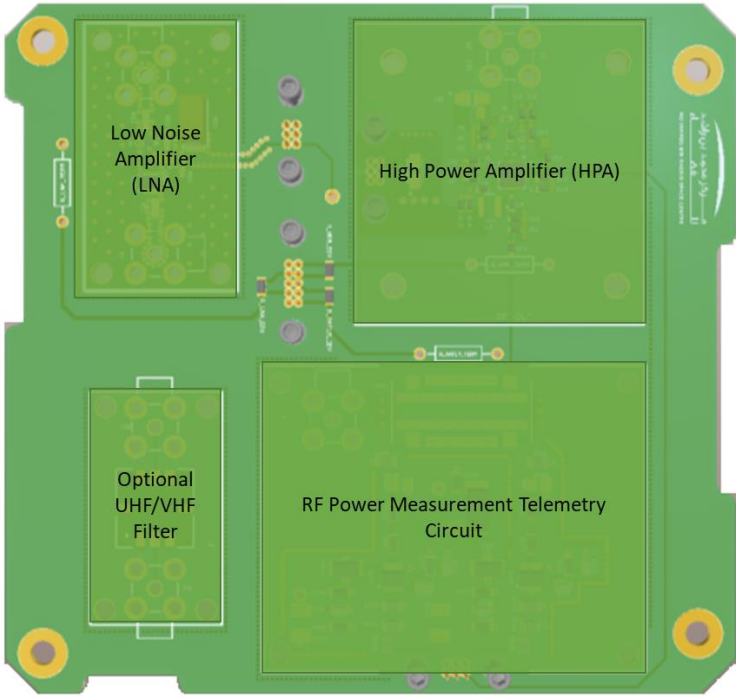

Fig. 5. RF Front End Board (Top View)

Fig. 6 below illustrates the bottom view of the RF front end. It contains the connectors assembly as well as a thermal pad for heat sink interface. The circuits are also isolated from one another via a ground plane underneath each PCB to make it easy to transfer the PCB design and reuse for different projects and also at the same time improve the signal integrity and noise immunity.

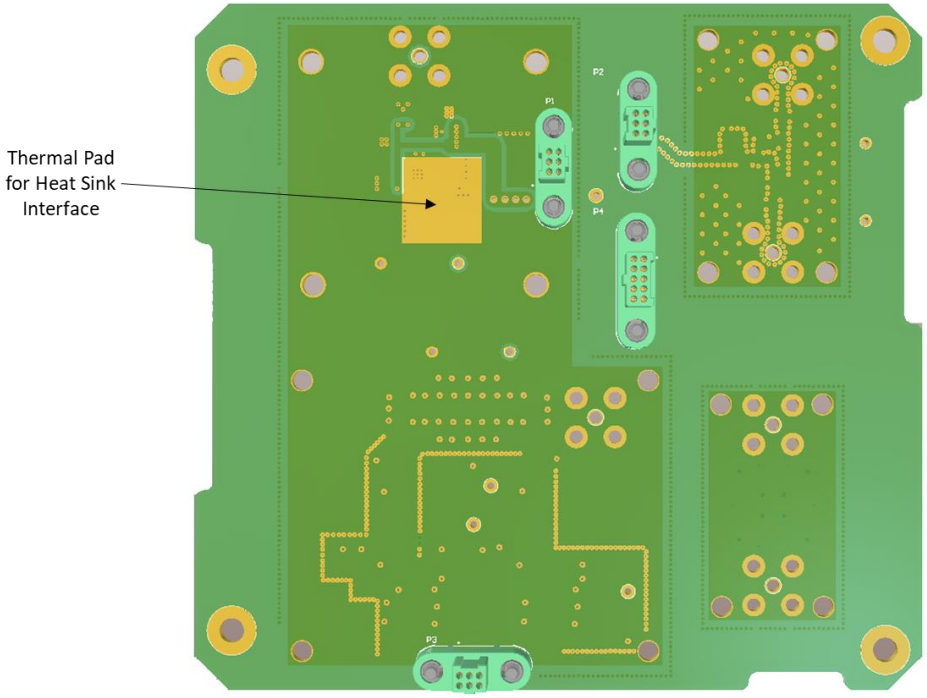

Fig. 6. RF Front End Board (Bottom View)

3. Results and Discussion

The system is tested across several phases of satellite development. The first phase is bench level testing of each board: the transceiver board and the RF front end board. Next, the two boards are integrated and tested together as an integration test. Moving forward, the integrated unit is tested in a thermal chamber environment to verify the system's performance across low and high temperature extremes as well as verify workmanship of the component soldering. Finally, the system is integrated onto the satellite interfaced together with the electrical power subsystem and command and data handling subsystem or in other words the on board computer (OBC) and tested as a full system with ground station electric support equipment.

During the bench test, each board is tested standalone. The tests performed on the transceiver board consist of power regulation check, SPI and I2C interface check, and finally RF output check. The RF output level of the transceiver transmitter is tuned to optimize the input to the high power amplifier (HPA) as an input to the RF front end board. Other tests performed on the transceiver include bandwidth occupancy, channel power measurements, constellation measurement, and error vector magnitude (EVM) measurement. Further, the tests performed on the RF front end include high power amplifier (HPA) RF output power measurement per value of input control voltage, low noise amplifier (LNA) performance, and finally power measurement telemetry circuit to obtain the coefficients for reading the RF output power telemetry. The same set of tests are conducted as a bench test, as an integrated unit, and as an integrated unit during thermal cycle testing and system integration test. The test results are summarized in the following sections.

3.1 Bench Test Result

Fig. 7 below illustrates the test result for the high power amplifier (HPA). For this test the input power is 0dBm supplied from a signal generator. The control voltage is varied directly using a power supply. The result shows expected results of the power amplifier.

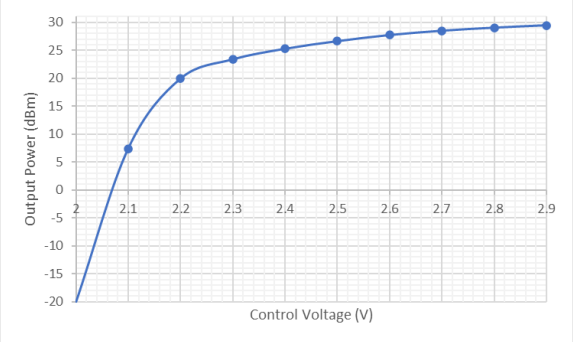

Fig. 7. RF Front End High Power Amplifier (HPA) Output (Pin=0dBm)

Fig.8 below illustrates the test result for the high power amplifier (HPA). For this test, the input power is 4.5dBm supplied from a signal generator. The value of 4.5dBm is chosen to provide optimal performance and output power from the high power amplifier (HPA). Similar to the result displayed in Fig. 7 above, the control voltage is varied directly using a power supply. The result shows expected results of the power amplifier.

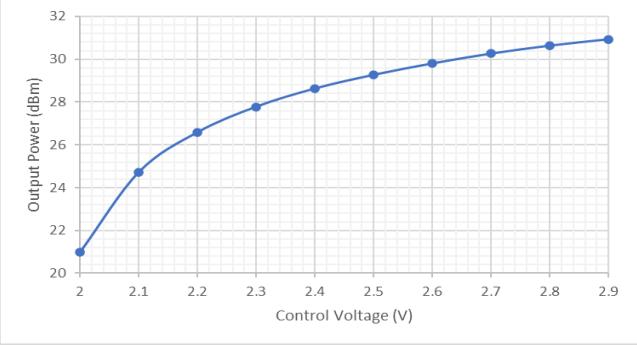

Fig. 8. RF Front End High Power Amplifier (HPA) Output (Pin=4.5dBm)

Next, the setup is changed and the control voltage is supplied from the output of a digital to analog converter (DAC). The DAC is controlled by command to output a voltage from 1.8V up to 3V in 0.1V steps and the RF output power is measured using a spectrum analyser. Fig. 9 below illustrates the results. The results are similar to that when the power supply is the source of the control voltage. The signal shows good integrity as well no indication of any interference due to any kind of noise.

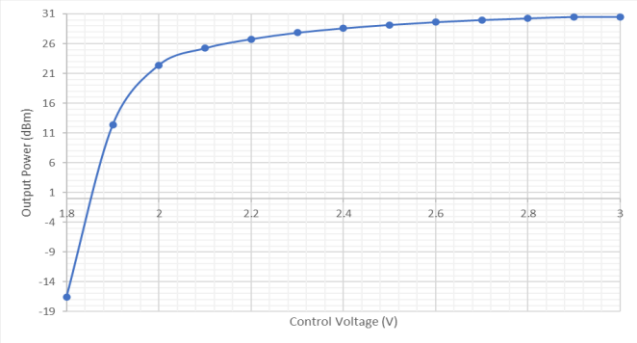

Fig. 9. RF Front End High Power Amplifier Output (DAC Control Voltage)

Fig. 10 below illustrates the results for the low noise amplifier (LNA). The sensitivity and gain flatness are checked for the low noise amplifier (LNA). The low noise amplifier (LNA) is tested with a signal level as low as -130dBm up to the value upon which the LNA saturates. The signal generator cannot generate a signal level lower than -130dBm, however, the LNA is verified with no issues for a signal level down to -130dBm. Nevertheless, the LNA saturates at -5dBm. This is not an issue since the uplink signal level is expected to be around -85dBm according to link budget analysis.

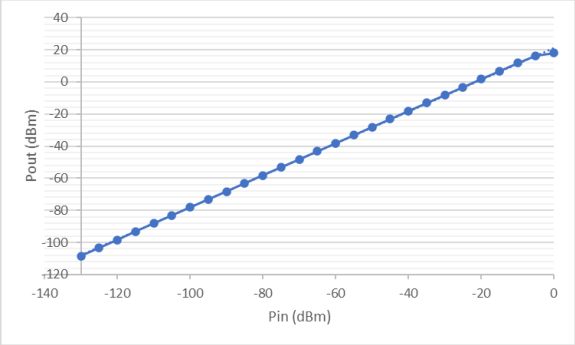

Fig. 10. Low Noise Amplifier (LNA) Sensitivity

Fig. 11 below illustrates the results for the gain of the low noise amplifier (LNA). The gain is maintained at around 21dBm up until the point at which the LNA saturates. The noise figure of the LNA is between 0.7~0.8dB.

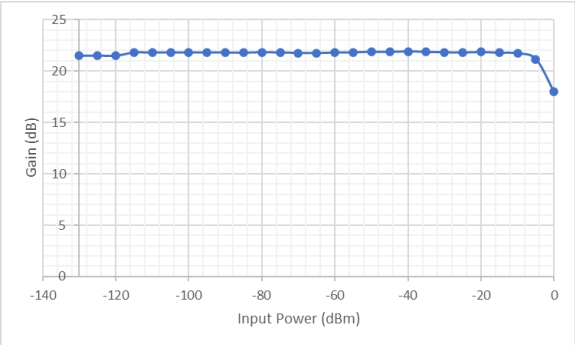

Fig. 11. Low Noise Amplifier (LNA) Gain Flatness

3.2 Integrated Unit Test Result

The integrated unit is shown below in Fig. 12 below. Table 2 below summarizes the test results for the integrated unit. The test is conducted at ambient test conditions, cold cycle, and hot cycle. The results are summarized in the figures and tables that follow.

Fig. 12. Integrated Unit

Table 2. Integrated Test Result Summary

Item	Test Result Summary
Frequency	UHF Downlink
Data Rate	9.6kbps
Modulation Scheme	BPSK
RF Output Power	30.8dBm
EVM	<10%
Data Sending and Receiving	Successful

As shown in Fig. 13 and Fig. 14 below, the BPSK constellation at the output of the transciever and RF front end integrated with the transceiver is as expected.

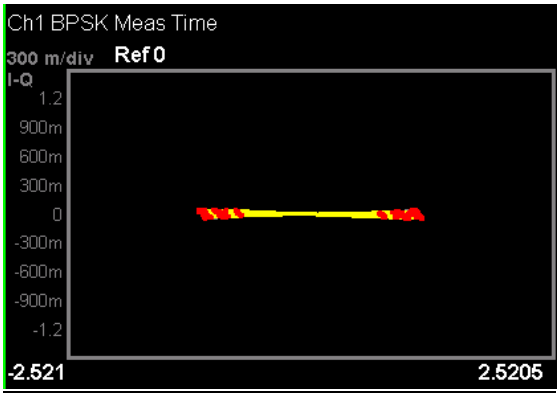

Fig. 13. Constellation Test Result at the output of the transceiver

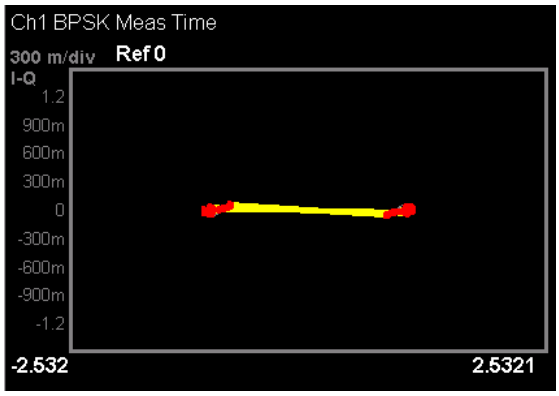

Fig. 14. Constellation Test Result at the output of the RF Front End

As shown in Fig. 15 and Fig. 16 below, the channel power at the output of the transciever and RF front end is as expected and meeting design requirements. As illustarted in section 3.1 above, the RF front end requires an input of around 4.5dBm for optimum high power amplifier (HPA) performance. The output of the transciever is tuned to 4.8dBm to consider losses due to interfacing RF cables. The output of the RF front end integrated with the transeiver is tuned up to 30.8dBm by selecting and setting a fixed reference control voltage for this application. The results shown below are at the output before the optional filter.

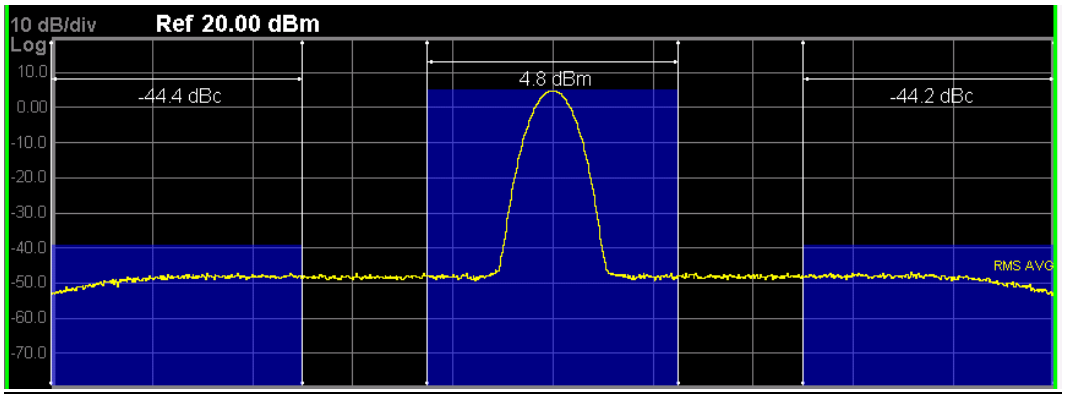

Fig. 15. Channel Power Test Result at the output of the transceiver

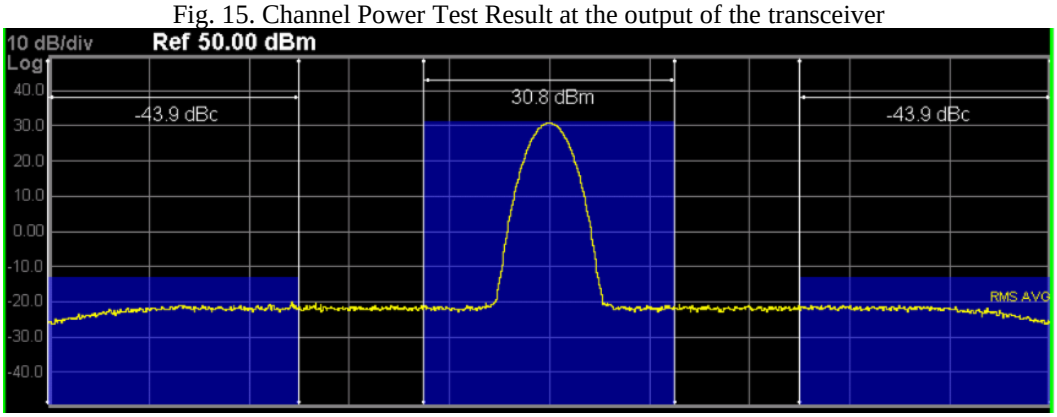

Fig. 16. Channel Power Test Result at the output of the RF Front End

Table 3 below summarizes the EVM test result at the output of the UHF transmitter and RF front end. The result is acceptable and below the required 10%. It is shown that the power amplifier does not increase the EVM. Further improvements can be done in the future to improve the EVM at the transceiver side.

Table 3. EVM Test Result

EVM Value at	Test Result
Transceiver Output	9.4147%
RF Front End Output	9.3578%

3.3 Thermal Cycle Test Result

Table 4 below summarizes the test results for the integrated unit tested in thermal cycle test environment. The test is conducted at ambient test conditions, cold cycle, and hot cycle. The results are summarized in the figures and tables that follow.

Table 4 Thermal Cycle Test Result Summary

Item	Test Result Summary
Frequency	UHF Downlink
Data Rate	9.6kbps
Modulation Scheme	BPSK
RF Output Power	30.6dBm
EVM	<10%
Data Sending and Receiving	Successful

As shown in Fig. 17 below, the BPSK constellation at the output of the integrated unit is as expected.

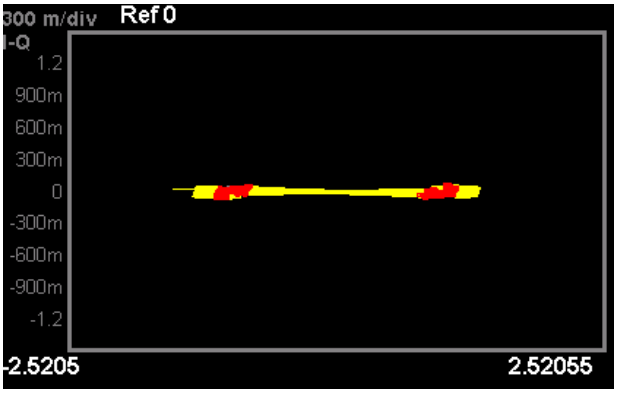

Fig. 17. Constellation Test Result at the output of the integrated unit

The output of the integrated unit during thermal cycle test is illustrated in Fig. 18, Fig. 19, and Fig. 20 below for ambient, cold cycle, and hot cycle test conditions, respectively.

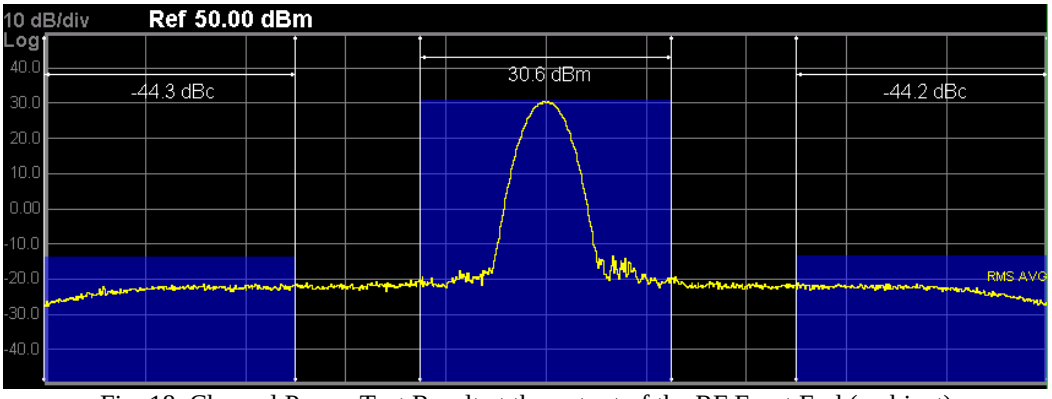

Fig. 18. Channel Power Test Result at the output of the RF Front End (ambient)

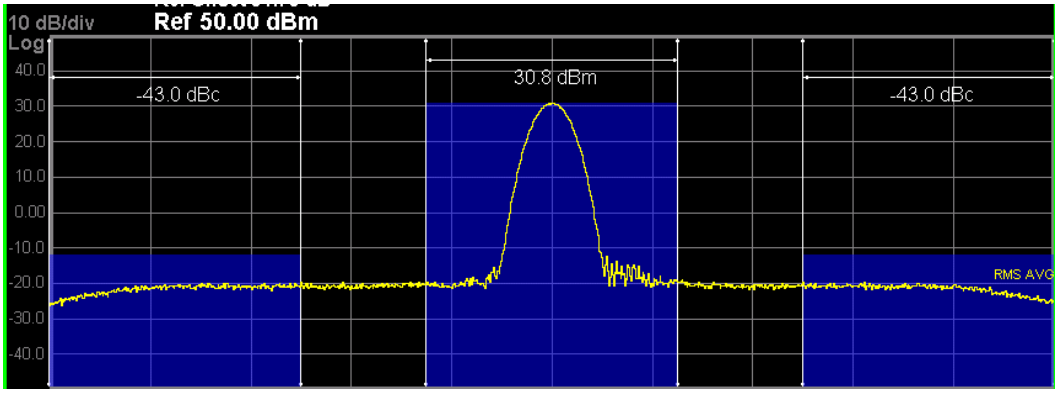

Fig. 19. Channel Power Test Result at the output of the RF Front End (Cold Cycle)

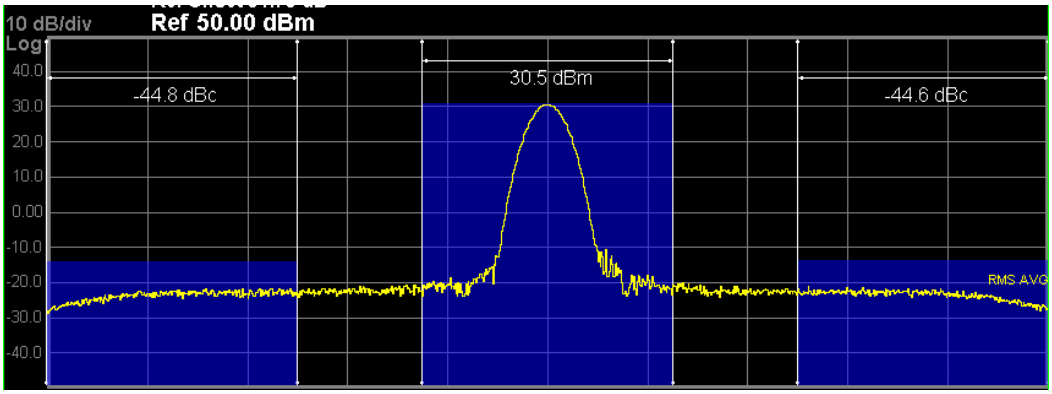

Fig. 20. Channel Power Test Result at the output of the RF Front End (Hot Cycle)

Table 5 below summarizes the EVM test result at the output of the integrated unit during thermal cycle test. The result is acceptable and below the required 10%.

Table 5. EVM Test Result

EVM Value at	Test Result
RF Front End Output	7.7987% at ambient
	9.0654% at cold cycle
	9.3285% at hot cycle

4. Design Optimization

The design is optimized and improved by incorporating a heat sink to the design. The benefits of adding a heat sink beneath the RF front end board, is particularly to dissipate the heat from the hottest and most power consuming component on the board, which is the high power amplifier (HPA). In general, heat sinks are required to prevent self-heating of the component from happening. The power dissipation at the junction causes the junction temperature to rise. As a result the current, and hence, the power dissipation increases. Eventually, this high power dissipation causes the component to self-heat and eventually get damaged, but also degrades the performance as a portion of the RF power output is lost as heat. Thus, the heat sink disposes of the excess heat [3]. Other than protecting the component from damage, the heat sink also improves the efficiency of the power amplifier, reduces its current consumption, and yields a higher RF output power [4]. This benefits the satellite in many ways such as power budget and link budget. From a power budget perspective, the power consumption of the unit is reduced when incorporating a heat sink. From link budget point of view, a higher RF output power results in a greater space to earth downlink link margin.

Before designing and manufacturing the heat sink, thermal analysis is conducted on the RF front end to assess its performance under worst hot temperature conditions. The test is performed by setting the interface temperature at 40°C, which serves as the boundary condition. A heat load of 5W is applied to the HPA region every 10 minutes for a cycle period of 96 minutes. The results of the test show that the maximum temperature reached by the HPA is

160°C, which is considered high in the absence of the heat sink. To address this issue, a heat sink is designed to reduce the HPA temperature to 64°C. Fig. 21 and Fig. 22 below demonstrate the analysis results in the cases without and with the heat sink.

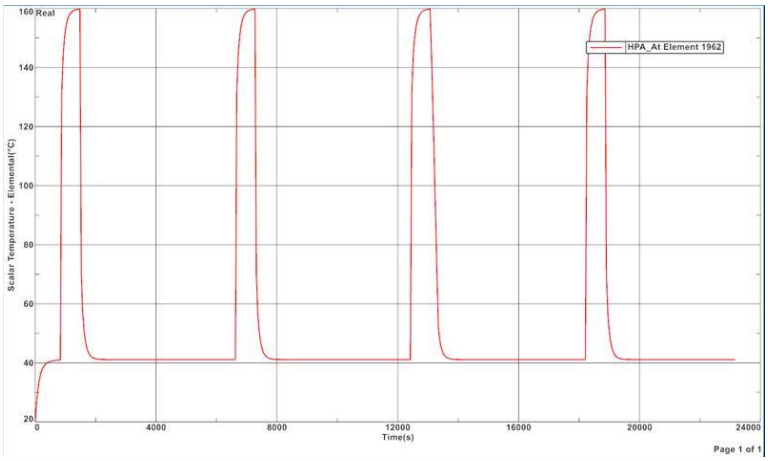

Fig 21 Thermal Analysis Result without Heat Sink

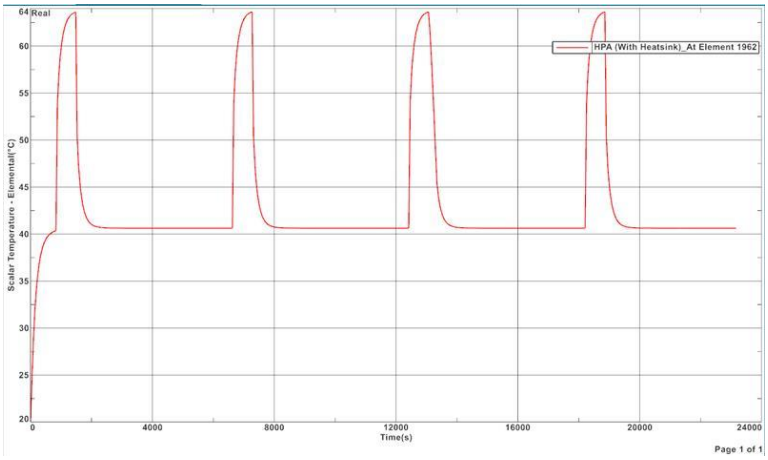

Fig 22. Thermal Analysis Result with Heat Sink

Fig 23. below shows an image of the heat sink from the bottom with the thermal interface material attached.

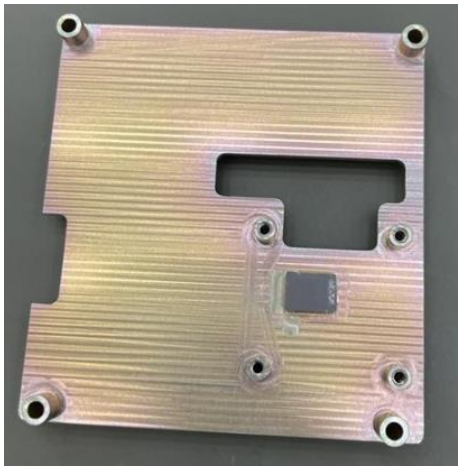

Fig 23. Manufactured Heat Sink

5. Conclusion

In conclusion, this paper summarizes the design, test, and optimization of a UHF downlink, VHF uplink satellite communication system suitable for cubesat applications. The paper illustrates the design in detail and well as documents the results on the bench test level, integration test levels, thermal cycle test levels. The design is also optimized by analysing, designing, and implementing a heat sink. Further work can be done to improve the performance of the system, enhance its modularity, and expand its applicability to higher commonly used frequency bands for low earth orbit satellite applications in the future.

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