

## A Ka Band High Data Rate Transmitter for LEO Satellites

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### Abstract

The paper presented at SpaceOps 2025 addresses the design of a Ka band high data rate transmitter for LEO satellites. This paper is especially focused on the RF & microwave sub-systems. The purpose of this transmitter is to operate the downlink from a LEO satellite to a ground station. High data rates are required to meet the expressed demand from a satellite operator to enable much more data volume downlink.

The Ka band transmitter comes as the latest generation of SOE (Satellite Onboard Electronics ex. Syrlinks) High-Data-Rate Transmitter dedicated to Nano/micro-satellites. It especially meets the expressed demand from a satellite operator to implement high data rate transmission between satellite and ground segment, enabling much more data volume downlink [1]. The equipment is a latest state-of-the-art qualified COTS based design. Such design is perfectly adapted to New-Space programs, where cost effectiveness, performances and reliability are success key factors. The allocated band goes from 25.5 to 27.0 GHz. Concerning the waveform the DVB-S2 standard is used [2] to get flexibility for the modulation (QPSK, 8PSK, 16APSK, 32APSK) and for the coding rate. Traditionally the X band from 8.025 to 8.0 GHz is used to ensure the downlink [3] but the available bandwidth is poor, only 375 MHz. Also, it is important to know the X band is starting to become saturated due to the increase in the number of users. This explains the growing interest in Ka band.

**Keywords:** Transmitter, Ka band, Satellites, Data rate, Downlink, DVB-S2

### 1. Introduction

The first part of the paper will present an overview of the transmitter architecture. A high-level bloc diagram will show the 4 main sub-systems: The base band sub-system, the power sub-system, the RF modulator sub-system and the Power Amplifier sub-system. The next paragraph will detail the RF modulator sub-system. We will see that a direct IQ conversion architecture was chosen. The following paragraph will talk about the Power Amplifier. Indeed, the SSPA is a major component for a RF transmitter. We will see that a 10 W packaged MMIC was selected; some measurements results will be presented. The last part of the paper will exhibit some first results and especially the BER vs Eb/N0 characteristics which are critical for the budget link.

The Ka band transmitter implements advanced encoding techniques and modulation schemes especially the DVB-S2 standard to achieve useful data rates of around 1 Gbps. One key feature is the capability to change and adapt the transmission parameters dynamically and in-flight. The following table sums up the targeted specifications.

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Table 1. Main specifications of the Ka band transmitter.

Specification	Value
Frequency band	25.5 to 27.0 GHz
Maximum RF output power	36 dBm ± 0.5 dB (4W)
Modulation & coding	DVB-S2 (QPSK, 8PSK, 16-APSK & 32-APSK)
Filtering	SRRC 0.35
Input data rate	up to 1200 Mbps
Interface	8 bits LVDS + clock
Output symbol rate	Up to 440 Msps
RF output interface	2.92 mm (coaxial)
Input voltage range	22 to 38 V dc
Power consumption	< 60 W
Size	184 mm x 206 mm x 69 mm
Mass	2,570 g
Operational temperature range	-20°C / +50°C
Life time	7 years LEO missions

## 2. Overview of the Ka band transmitter

The Ka band transmitter consists of 4 main sub-systems:

- The Base Band sub-system.
- The Power sub-system
- The RF-modulator sub-system
- The Power Amplifier sub-system

These sub-systems are described figure 1.

A key point is that we have chosen to work with a direct conversion architecture; The base band signals (I&Q) are directly converted to Ka band. This choice allows to simplify the schema, to minimize the components number and to simplify the filtering. The difficulty is to get an IQ modulator with the required performances even if some corrections can be made by the digital signal processing (IQ imbalance corrections).

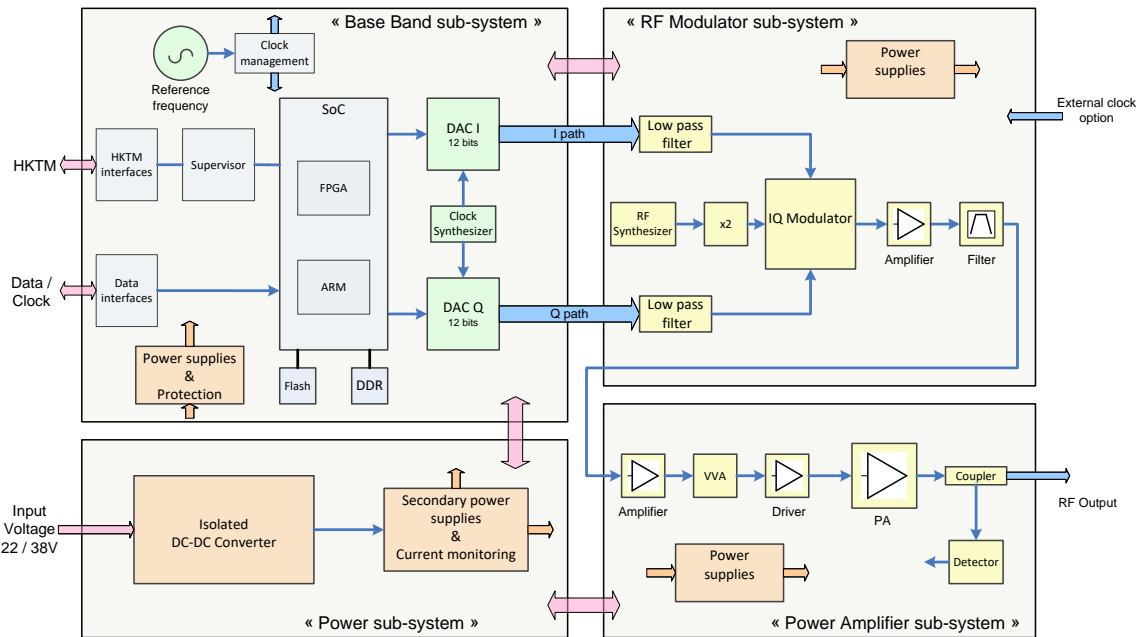


Fig. 1. High level bloc diagram of the Ka band transmitter

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The Power sub-system integrates a galvanic isolation primary DC-DC converter. Its output voltage is defined by the PA drain voltage requirement; Today +20V is baselined but it may change slightly depending on the tests carried out on the SSPA evaluation module. A trade off will have to be chosen between the RF output power, the power consumption, and the junction temperature if we want to remain in line with the ECSS derating rules.

Backstream there are 2 secondary DC-DC converters to generate the following voltages: 5,5 V and 3,8 V. Then several LDO regulators will be used to provide the different voltages for each component.

The main functions of the Base Band subsystem are the SoC, the FPGA (Supervisor), the interfaces, the RAM, the non-volatile memory, the Digital to Analog Converters, the clock management and so on.

These functions allow to control and command the equipment and to proceed with the Digital Signal Processing tasks (input data management, encoding, modulation, flow control, ...). Moreover, the 2 DACs allow to generate the I signal and the Q signal for the RF modulator. For 360 Msps the over-sampling is 4, that means the DAC clock frequency is 1440 MHz. For 440 Msps the over-sampling is 3, then the DAC clock frequency is 1320 MHz. The variable over-sampling rate is explained by the fact that the DAC clock frequency is limited to 1.5 GHz.

The RF modulator sub-system is used to transpose the I&Q base band signal to the wanted carrier between 25,5 and 27 GHz. For that, the IQ modulator needs a Local Oscillator (LO). Firstly, this LO is generated thanks to a RF synthesizer at a frequency of around 13 GHz. Then this frequency is multiplied by 2 with a doubler to reach the selected carrier at around 26 GHz. Obviously, this frequency is fully programmable with a fine step. At the end of this RF chain, we have an amplifier to increase the output power level and a filter to limit the out of band noise and the possible spurious.

The last sub-system is the solid-state power amplifier (SSPA). This is an important function because it is essential to obtain the wanted RF output power level for the budget link. This is also important because the SSPA often constitutes the main part of the equipment power consumption (around 80%).

To build this SSPA several amplifier stages are used. Moreover, an Automatic Level Control (ALC) loop is integrated inside the design to stabilize the output level over temperature, over the time and over the load. This ALC loop is realized with a directive coupler, a RF detector, a Voltage Variable Attenuator (VVA), a DAC and an ADC. With these blocks the FPGA can control the loop by using a PI type algorithm.

### 3. The RF Modulator sub-system

One of the main components of the RF Modulator Sub-System is the frequency synthesizer that shall generate an LO around the range of 13 GHz. To fulfill this function a biCMOS SiGe ASIC was selected, it integrates a PLL and some VCOs. For the reference frequency the base band part provides a 40 MHz clock from an internal OCXO. In these conditions the integrated phase error reaches 0.6°rms @ 13 GHz (from 100 Hz to 10 MHz).

At the synthesizer output we find a MMIC amplifier and some attenuators to generate the wanted level at the frequency doubler input (+3 dBm is required). The frequency doubler is an active MMIC (GaAs pHEMT) and it can provide up to +15 dBm of RF output power at the harmonic 2. This feature eliminates the need of an amplifier between the doubler and the IQ mixer.

The IQ mixer is MMIC that can work from 24 to 28 GHz, it needs a LO drive of +10 dBm. This MMIC utilizes two double balanced mixer cells and a 90-degree hybrid fabricated in a GaAs Schottky diode process. Its typical image rejection is 21 dB without digital optimization. Indeed, some Digital Signal Processing techniques allow to correct the gain and the phase imbalances. A calibration is performed by optimizing the EVM performance. In the same way we have used a compensation method to optimize the LO leakage. This well-known method consists of injecting a DC offset voltage on the I and Q paths. About the conversion loss, with 500 mVpeak-peak on I & Q inputs, we get a modulated signal of -10 dBm at the RF output at 26 GHz.

The I & Q inputs need a low pass filter to reject the various unwanted signals from the DACs outputs especially the 2nd and the 3rd Nyquist zone. These filters are chosen to not bring group delay variation inside the useful bandwidth. For example at 400 Msps the useful bandwidth is 270 MHz knowing a SRRC filter with a roll off of 0.35 is used :  $0.5 R_s (1+0.35) = 270 \text{ MHz}$ .

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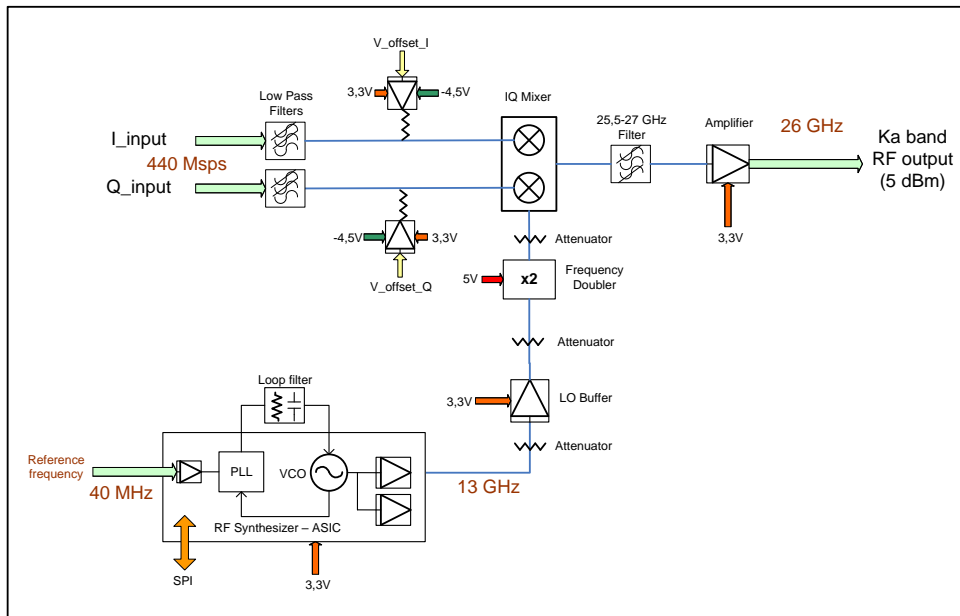


Fig. 2. Bloc diagram of the RF modulator sub-system

At the IQ mixer output a pass band filter is used. This filter is broadband [25-27.5 GHz] to not bring group delay variation inside the band from 25.5 to 27 GHz. The filter shall reject the out of band noise and the possible spurious at 13 GHz and at 39 GHz (H3 of 13 GHz). The filter is designed to a ceramic substrate with a thin film process to get a fine resolution and to reduce the form factor. The filter size is only 5.5 mm x 2.3 mm. Its insertion loss is around 3 dB.

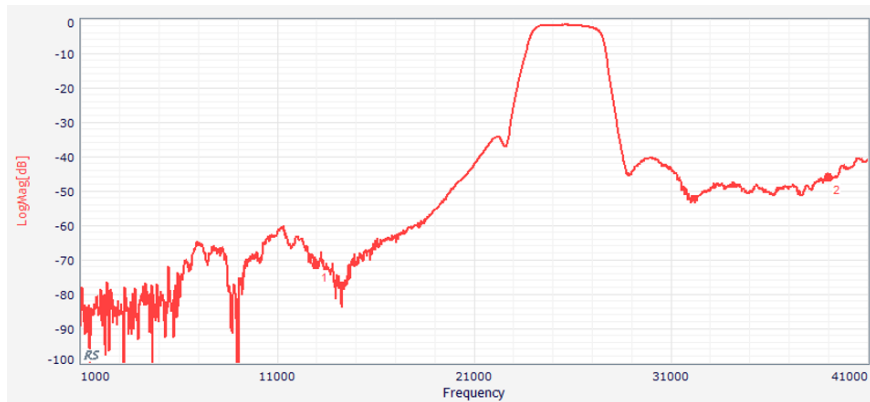


Fig. 3. Wideband response of the pass band RF filter

The last RF component of the modulator sub-system is a Ka band low power amplifier. A broadband MMIC (GaAs pHEMT) was selected [18-31 GHz], it owns the following characteristics: Single bias operation (to avoid the need of a negative gate voltage), flexible supply voltage (from +3.3 to +5V), flexible P1dB and OIP3 (an external resistor allows to adjust the bias current). Its typical gain is quite stable over our band : +22 dB at the beginning and +21 dB at the end of the band. This amplifier allows to get an output power from 0 dBm to +10 dBm according to the level on the I&Q inputs.

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A PCB of the overall RF modulator was built in order to check if the expected results were reached. Firstly, we have measured the output spectrum and the output power for various I&Q input voltages. The selected waveform is a 8PSK (without coding, with SRRC 0.35 filtering) at 360 Msps. At 500 mV<sub>peak-peak</sub> the output power at 26 GHz is +8 dBm. In these conditions the 99% occupied bandwidth (OBW) reaches 410 MHz (Figure 3). If we increase the input level the linearity degrades and the OBW and the Error Vector Magnitude (EVM) increases. That is explained by the fact that we are approaching the amplifier P1dB; Also, the linearity of the IQ mixer has some limits.

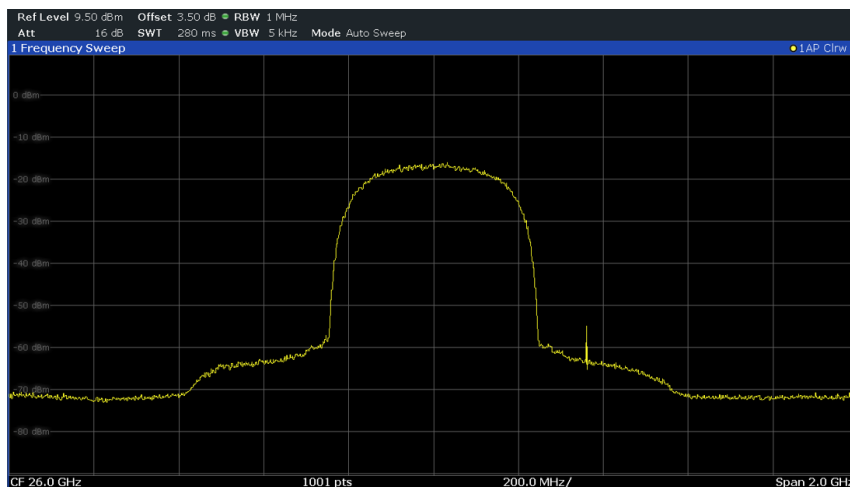


Fig. 4. Output spectrum of the RF modulator (8PSK SRRC 0.35 ; 360 Msps – 26 GHz)

To get a good idea of the modulator performances, it is important to perform some EVM measurements. An example is provided below with a 8PSK waveform at 360 Msps. We can see below the IQ constellation. In these conditions the EVM<sub>RMS</sub> reaches 4.2%. This value is in line with our expectations. To improve this performance, we have the possibility to use an external high quality 100 MHz reference clock for the RF synthesizer. With this clock the phase noise of the local oscillator at 13 GHz is improved (0.3°<sub>rms</sub> instead of 0.6°<sub>rms</sub>) and the EVM<sub>RMS</sub> is reduced to 3.5%.

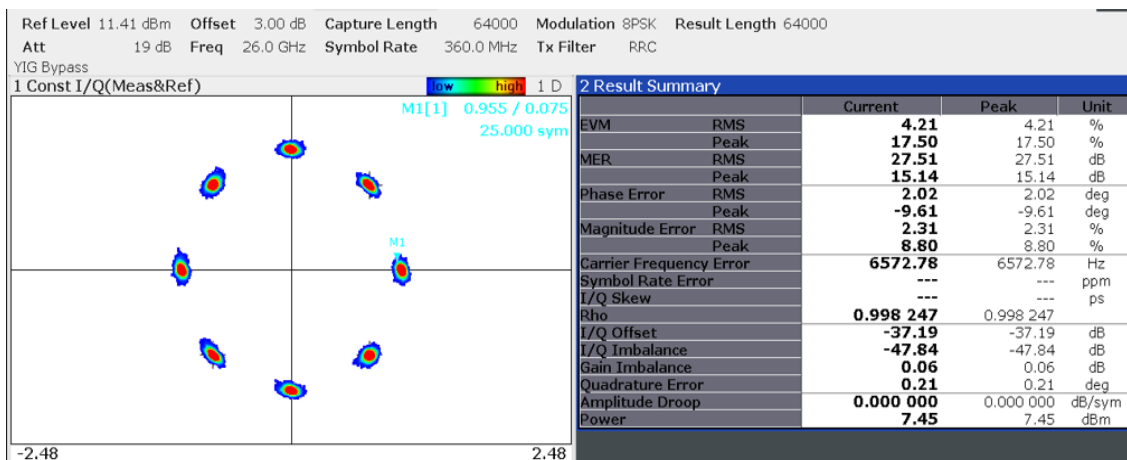


Fig. 5. EVM of the RF modulator (8PSK SRRC 0.35 ; 360 Msps – 26 GHz)

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#### 4. The Power Amplifier sub-system

As it was already mentioned, the SSPA is a major function for a transmitter. A trade off shall be determined between the linearity (i.e. EVM) and the power consumption. Our RF budget link shows we need 4W at the transmitter output. To realize this, we have selected a packaged MMIC with the following characteristics:

- Frequency range: 25.5 to 27 GHz
- Operating conditions:  $V_d = 20\text{ V}$ ;  $I_{dq} = 900\text{ mA}$
- Small signal gain: 27 dB
- Power gain: 14 dB @  $P_{sat}$
- Saturated output power: 40.5 dBm @ 25°C
- Power added efficiency: 24% @  $P_{sat}$  / 25°C
- Package metal/ceramic: ~10 mm x 12 mm x 2 mm

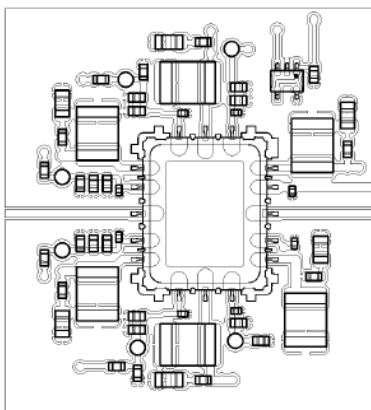
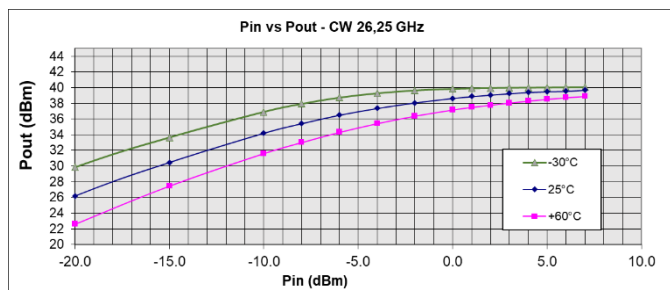


Fig. 6. Ka band Power Amplifier integrated on a PCB

The device is compliant with ECSS-Q-ST-30-11C derating rules and is manufactured on a technology successfully evaluated for space use and referenced in the European Preferred Part List (GaN on SiC, 0.15  $\mu\text{m}$  pHEMT). It is also interesting to mention that a copper coin PCB technology is used to assemble this PA. Indeed, the thermal management is always a complex problem with this level of power and at these frequencies.

Before the last stage, a driver amplifier is mandatory to feed properly the PA. It is important to carefully choose the driver because if its output power is too weak then the driver may enter in its compression area. But if the selected driver owns a too high compression level, the power consumption of the system will be penalized. We have selected a three stage GaAs MMIC producing 2 Watt output power under +6V. The circuit is manufactured with a pHEMT process 0.15  $\mu\text{m}$  gate length. It can work inside the [21-28 GHz] band and owns a gain of around +20 dB. It is packaged inside a 6 mm x 5 mm case.

Thanks to breadboards, the performance of the PA with the driver could be tested over the temperature (Figure 7). The small signal gain reaches 42.5 dB at +60°C and 50 dB at -30°C. The saturated power is in the range from 38.5 dBm to 40 dBm according to the temperature. This saturated power is reached with a gain of around 35 dB. The PAE oscillates between 16% at hot and 20% at cold, these values take into account the driver power consumption. All the results are not de-embedded in the component plane but are obtained at the coaxial connector level.



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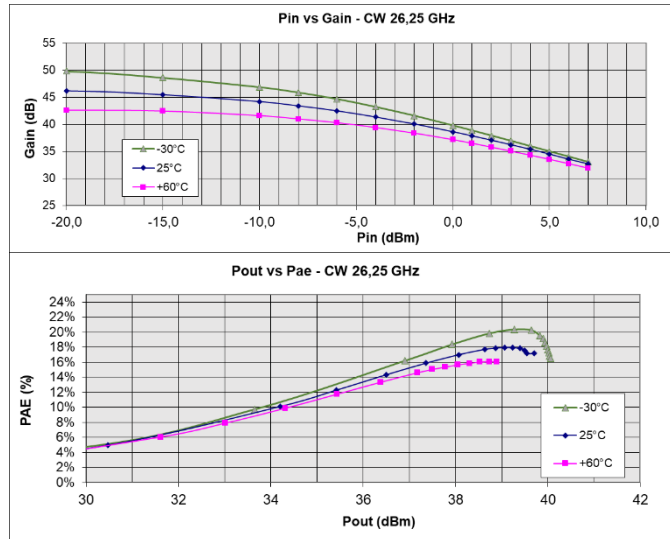


Fig. 7. Ka band SSPA performances over temperature

## 5. First system test

An important measurement to validate the architecture of this Ka band transmitter is to get the BER as a function of the  $E_b/N_0$ . With this curve we can get the implementation losses. It is enough to compare the result with the theoretical curve for a given modulation and coding. To perform the BER measurement we use a CORTEX 4G from Safran Data Systems, this is a high data rate receiver that needs an IF frequency of 1200 MHz to demodulate the signal. A downconverter is used to translate the signal from 26 GHz to 1.2 GHz. Also, the Cortex HDR owns a programmable noise source in order to sweep the  $E_b/N_0$ . Indeed, different noise levels are added to the signal with a power combiner to reach various BER values typically from  $10^{-3}$  to  $10^{-10}$ .

To compute the BER we use for data a PRBS 15 sequence. For the waveform we have used a QPSK with no coding but with a SRRC 0.35 filtering like the DVB-S2. To perform the test, we have associated the RF modulator breadboard with the PA and the driver. Another important point to note is that the CORTEX 4G owns a DEAF feature. The DEAF is a Digital Equalizer Automatic Filter, that allows to correct specific imperfections of the RF channel such as group delay variations or amplitude variations inside the bandwidth. Mainly the DEAF allows to improve the BER. Generally, we perform the BER measure with and without the DEAF option.

A result for an output back off of 1 dB (+38.5 dBm) is presented Figure 7. For a BER equal to  $10^{-6}$  the implementation loss is 2 dB without DEAF and lower than 0.75 dB with the DEAF. These results meet our expectations knowing this loss includes also the receiver loss. We can note the DEAF feature allows to win more than 1 dB on the budget link.

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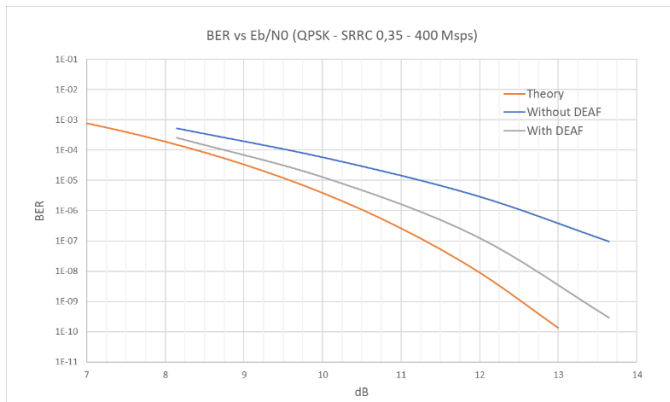


Fig. 8. Ka band transmitter BER vs Eb/N0 performances (QPSK without coding – 38.5 dBm – 26 GHz)

The next step will be to check the implementation loss with a DVB-S2 Modcod and especially with the Modcod 8 PSK<sup>9/10</sup>. Indeed, with this Modcod at 400 Msp/s the user data rate exceeds 1 Gbps which is quite interesting.

A final result which may be interesting to present is an EVM measurement in 32-APSK [4] at the SSPA output for 4W at 360 Msp/s (Figure 9). In these conditions the raw data rate is 1.8 Gbps. Obviously, the non-linearity inherent to the SSPA degrades the EVM<sub>RMS</sub> value but the result remains acceptable with 10.5%. The EVM<sub>RMS</sub> value may be also used to compute the BER performance versus the Signal to Noise Ratio [5]. In addition, various EVM<sub>RMS</sub> results are summed up inside Table 2.

About the 1.8 Gbps we can add the data are generated inside the FPGA, indeed our LVDS interface is for now limited to 1.2 Gbps. But we are working on different options such as DDR (Double Data Rate) mode, 16-bits LVDS and ethernet to accept higher input data rate from a mass memory.

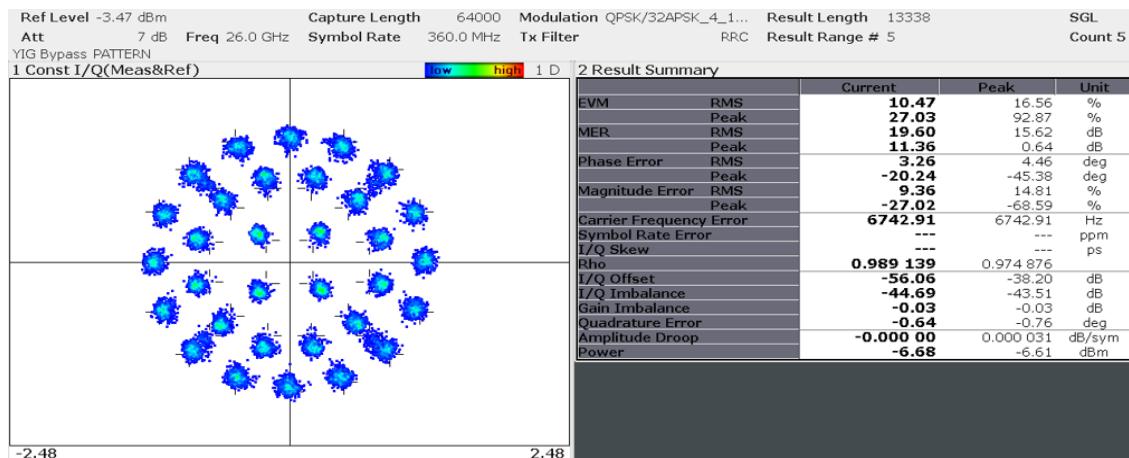


Fig. 9. Ka band transmitter EVM performances (32-APSK - 360 Msp/s – 36 dBm – 26 GHz)

Table 2. Some EVM<sub>RMS</sub> results at 36 dBm / 26 GHz (Transmitter output)

<b>Modulation / ModCod</b>	<b>@ 360 Msps</b>	<b>@ 440 Msps</b>
QPSK / ModCod 11	5.3 %	6.1 %
8PSK / ModCod 17	5.7 %	6.8 %
16-APSK / ModCod 23	8.4 %	8.7 %
32-APSK / ModCod 28	10.5 %	10.7 %

## 6. Conclusion

In this paper we have depicted the design of a high data rate Ka band transmitter for satellites in LEO orbits. Some specific focuses were done about the microwave sub-assemblies and the RF chain. We have seen that the transmitter is able to provide high symbol rates (up to 440 Msps and more) with a high RF output power (4 W). Also, it is important to mention that this transmitter is intended to operate with the DVB-S2 standard. For those who might be interested, the commercial name of this equipment is KaLLISTO and Engineering Models (EM) may be available as early as Q3 2025. About the next steps, we plan to upgrade this product with at least a second channel to allow higher data rate and we will also begin to work on digital predistortion technics to compensate the effects of the SSPA non-linearities. This future feature should make it possible to improve the EVM and to reduce the ACPR (Adjacent Channel Power Ratio) levels. Another step will be to provide a waveguide output (WR34) to let the possibility to use a low loss waveguide filter and a waveguide isolator.

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